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④半導体装置の製造方法

⑳特　　願 昭57—7933
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⑫発 明 者 松村学
川崎市幸区堀川町72番地東京芝浦電気株式会社堀川町工場内

⑫発 明 者 前口賢二
川崎市幸区堀川町72番地東京芝浦電気株式会社堀川町工場内

⑪出 願 人 東京芝浦電気株式会社
川崎市幸区堀川町72番地

⑭代 理 人 弁理士 鈴江武彦　外2名

明　細　書

1. 発明の名称

半導体装置の製造方法

2. 特許請求の範囲

絶縁基板上にシリコン層を形成する工程と、該シリコン層上に互いに重なるシリコンパターン及び耐酸化性膜パターンを第1の酸化膜を介して形成する工程と、該耐酸化性膜パターンの一部を選択的に除去する工程と、酸化性雰囲気中で熱処理を施すことにより第1の酸化膜が露出した前記シリコン層領域に前記絶縁基板に達する第2の酸化膜を、シリコンパターンが露出した領域に少なくとも前記第1の酸化膜に達し、前記絶縁基板に達しない第3の酸化膜を夫々形成する工程とを具備したことを特徴とする半導体装置の製造方法。

3. 発明の詳細な説明

発明の技術分野

本発明は絶縁基板上に形成される半導体装置の製造方法に関する。

発明の技術的背景とその問題点

絶縁基板上に形成される半導体装置は例えばSOS (Silicon on Sapphire) 構造として知られている。

例えばnチャネルSOS/MOSトランジスタは第1図(a)(b)に示す如き構造を有している。図中1はサファイア基板であり、このサファイア基板1上にはフィールド酸化膜2によって電気的に分離されたp型単結晶シリコン層が形成されている。このシリコン層にはn⁺型のソース，ドレイン領域3，4が設けられている。これらソース，ドレイン領域3，4間の半導体基部5上にはゲート酸化膜6を介してゲート電極7が設けられている。

上述したSOS/MOSトランジスタでは動作時において半導体基部5が電気的に浮遊状態であるため、その電位がゲート及びp－n接合を介してのキャパシタンス・カップリングによって変動し、回路特性に悪影響を及ぼす。

そこで第2図(a)～(e)に示す如き方法により半

導体基部の電位を固定することが行われている。まず、サファイア基板11上にn型単結晶シリコン層12を形成する。次にこのシリコン層12上にシリコン窒化膜パターン13を形成する（第2図(a)図示）。この際、Si_3N_4膜パターン13とシリコン層12との間に酸化膜を設けることもある。次に、露出したシリコン層12をエッチングして最初の厚さの半分程度にまで減少させる（第2図(b)図示）。次に、シリコン窒化膜パターン13の一部を選択的にエッチング除去する（第2図(c)図示）。次に、酸化性雰囲気中で熱処理を施すことによりシリコン層12を一部エッチング除去した領域ではサファイア基板11に達する素子分離のための第1の酸化膜14を、シリコン窒化膜パターン13の一部をエッチング除去した領域ではサファイア基板11に達しない第2の酸化膜15を夫々形成する（第2図(d)図示）。次いで、シリコン窒化膜パターン13を除去する。つづいて、露出したシリコン層12表面に薄い熱酸化膜を形成し、

全面に例えばリンドープ多結晶シリコン膜を堆積する。つづいて、この多結晶シリコン膜をパターニングしてゲート電極16を形成し、このゲート電極16をマスクとして前記熱酸化膜をエッチングしてゲート酸化膜17を形成する。つづいて、n型不純物、例えばリンをイオン注入して図示しないソース，ドレイン領域を形成する。つづいて、全面にCVD-SiO_2膜18を堆積し、コンタクトホール19…を開孔した後、全面にAl膜を蒸着し、このAl膜をパターニングしてAl配線20…を形成してnチャネルSOS／MOSトランジスタを製造する（第2図(e)図示）。

以上のような方法でSOS／MOSトランジスタのソース，ドレイン領域間の半導体基部21を配線となる第2の酸化膜15下のシリコン層（配線層）22及び基部取出し領域23を通して外部電極に接続することができ、その電位を固定することができる。

ところで、近年半導体素子の高密度化に伴いサファイア基板上のシリコン層の厚さは次第に

薄くなりつつあり、0.6 μm以下の薄いシリコン層を使用する傾向にある。このように薄いシリコン層を使用するようになってくると、上述した従来方法では酸化性雰囲気中での熱処理工程で第2の酸化膜15とサファイア基板11との間に配線となるシリコン層22を残存させることが困難となり、また残存するシリコン層22は厚さが薄いため、その抵抗値が高くなるという問題点がある。

発明の目的

本発明は半導体素子の高密度化に伴って絶縁基板上のシリコン層が薄くなる傾向に対応しつつ、半導体基部の浮遊状態を解消して回路特性を向上した半導体装置の製造方法を提供することを目的とするものである。

発明の概要

本発明は以下の工程を具備することを特徴とする。

まず、絶縁基板上にシリコン層を形成した後、このシリコン層上に互いに異なるシリコンパターン及び耐酸化性膜パターンを第1の酸化膜を介して形成する。ここに用いる絶縁基板としてはサファイア、スピネル、二酸化シリコン等の酸化膜、シリコン窒化膜等が挙げられる。また、シリコンパターンとして用いられるシリコンは単結晶でも、多結晶でも、非晶質のものでもよい。また耐酸化性膜としてはシリコン窒化膜、Al_2O_3膜等が挙げられる。

次に、耐酸化性膜パターンの一部を選択的に

除去した後、酸化性雰囲気中で熱処理を施すことにより第1の酸化膜が露出した前記シリコン層領域に前記絶縁基板に達する第2の酸化膜を、シリコンパターンが露出した領域に少なくとも前記第1の酸化膜に達し、前記絶縁基板に達しない第3の酸化膜を夫々形成する。

第3の酸化膜が形成される領域では、素子分離のための第2の酸化膜が形成される領域よりも、シリコンパターンの厚さだけ酸化されるシリコンの厚さが厚い。このため絶縁基板上のシリコン層の厚さが薄くなっても第3の酸化膜と絶縁基板との間に充分厚いシリコン層を残存させることができる。したがって、この残存したシリコン層を配線として利用することによって、ソース、ドレイン領域間の半導体基部の電位を固定でき、回路特性を向上させることができる。

発明の実施例

本発明をnチャネルSOS/MOSトランジスタの製造に適用した一実施例を第3図(a)～(f)、第4図及び第5図を参照して説明する。

まず、サファイア基板31上に厚さ4000Åのp型単結晶シリコン層32をエピタキシャル成長させた。次に、このシリコン層32上に厚さ500Åの第1の酸化膜33、厚さ3000Åの多結晶シリコン層34及び厚さ2000Åのシリコン窒化膜35を順次形成した（第3図(a)図示）。

次いで、写真蝕刻法により前記シリコン窒化膜35及び多結晶シリコン層34の一部を選択的に順次除去して、シリコン窒化膜パターン36及び多結晶シリコンパターン37を形成し、第1の酸化膜33の一部を露出させた（第3図(b)図示）。

次いで、写真蝕刻法により前記シリコン窒化膜パターン36の一部を選択的に除去して、多結晶シリコンパターン37の一部を露出させた（第3図(c)図示）。

次いで、酸化性雰囲気中で熱処理を施した。この際、第1の酸化膜33が露出した前記シリコン層32領域に前記サファイア基板31に達する第2の酸化膜38が、多結晶シリコンパターン37が露出した領域に少なくとも前記第1の酸化膜33に達し、サファイア基板31には達しない第3の酸化膜39が夫々形成された。この時、第3の酸化膜39下のシリコン層32にはp型不純物、例えばボロンがイオン注入してあり、配線となる低抵抗のp⁺型不純物層40も形成される。（第3図(d)図示）

次いで、シリコン窒化膜パターン36、多結晶シリコンパターン37及び第1の酸化膜33を順次除去した後、露出したシリコン層表面に薄い熱酸化膜を形成した。つづいて、全面に例えばリンドープ多結晶シリコン膜を堆積し、この多結晶シリコン膜をパターニングしてゲート電極41を形成した。つづいて、ゲート電極41をマスクとして前記熱酸化膜をエッチングしてゲート酸化膜42を形成した。この際、ゲート電極41が形成されるシリコン層領域以外の、第2の酸化膜38と第3の酸化膜39間の熱酸化膜も除去され、同酸化膜38，39間のシリコン層32領域が露出した（第3図(e)図示）。

次いで、素子形成領域以外にホトレジストパターンを被覆し、このホトレジストパターン及び前記ゲート電極41をマスクとしてn型不純物、例えばリンをイオン注入してn⁺型のソース、ドレイン領域43，44及びソース、ドレイン領域間の半導体基部45を形成した。つづいて、第2の酸化膜38と第3の酸化膜39間のシリコン層32領域以外にホトレジストパターンを被覆してp型不純物、例えばボロンをイオン注入してp⁺型の基部取出し領域46を形成した。つづいて、全面にCVD－SiO_2膜47を堆積し、コンタクトホール48を開孔した後、全面にAl膜を蒸着し、このAl膜をパターニングしてゲート電極41のAl配線49及び基部取出し領域46のAl配線50を形成し、nチャネルSOS/

MOSトランジスタを製造した（第3図(f)、第4図及び第5図図示）。なお、第4図は第3図(f)の平面図、第5図は第4図のV－V線に沿う断面図である。

しかして、上記方法によればサファイア基板31上に設けられるシリコン層32の厚さが4000Åと非常に薄いにもかかわらず、第3の酸化膜39とサファイア基板31との間に配線となる充分厚いp⁺型不純物層40を残存させることができる。このため、p⁺型不純物層40及び基部取出し領域46を通して、ソース、ドレイン領域43，44間の半導体基部45を低抵抗で外部に取出すことができ、その電位を固定することができるので回路特性を向上させることができた。しかも、配線となるp⁺型不純物層40上の第3の酸化膜39は厚いので、この上の配線とシリコン層との間の浮遊容量は小さくなり伝播速度等の回路特性が悪化することはない。

なお、本発明は上記実施例の如くSOS構造の

膜パターン、37…多結晶シリコンパターン、38…第2の酸化膜、39…第3の酸化膜、40…p⁺型不純物層（配線）、41…ゲート電極、42…ゲート酸化膜、43，44…ソース，ドレイン領域、45…半導体基部、46…基部取出し領域、47…CVD－SiO_2膜、48…コンタクトホール、49，50…Al配線。

出願人代理人　弁理士　鈴　江　武　彦

半導体装置に限らず、三次元回路素子の如くSiO_2膜上のシリコン層に半導体素子を形成する場合にも同様に適用できる。

発明の効果

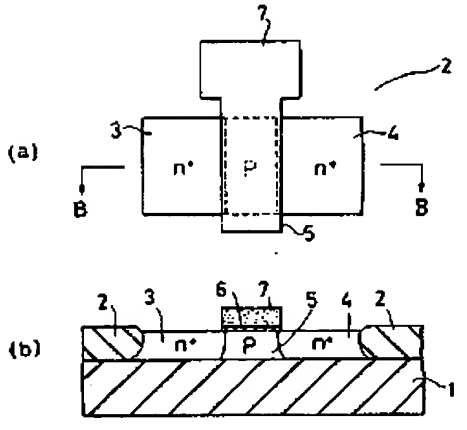
本発明によれば半導体素子の高密度化に伴って絶縁基板上のシリコン層が薄くなる傾向に対応しつつ、半導体基部の浮遊状態を解消して回路特性を向上した半導体装置の製造方法を提供できるものである。

4.図面の簡単な説明

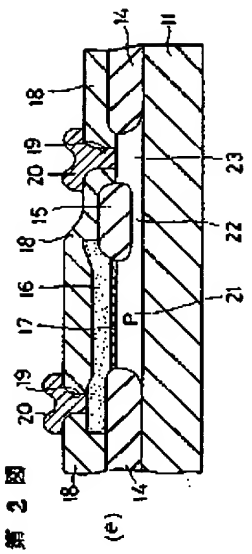
第1図(a)は従来のSOS/MOSトランジスタの平面図、同図(b)は同図(a)のB－B線に沿う断面図、第2図(a)～(e)は従来の半導体基部の電位を固定したSOS/MOSトランジスタの製造方法を工程順に示す断面図、第3図(a)～(f)は本発明の実施例におけるSOS/MOSトランジスタの製造方法を工程順に示す断面図、第4図は第3図(f)の平面図、第5図は第4図のV－V線に沿う断面図である。

31…サファイア基板、32…p型シリコン層、39…第1の酸化膜、36…シリコン窒化

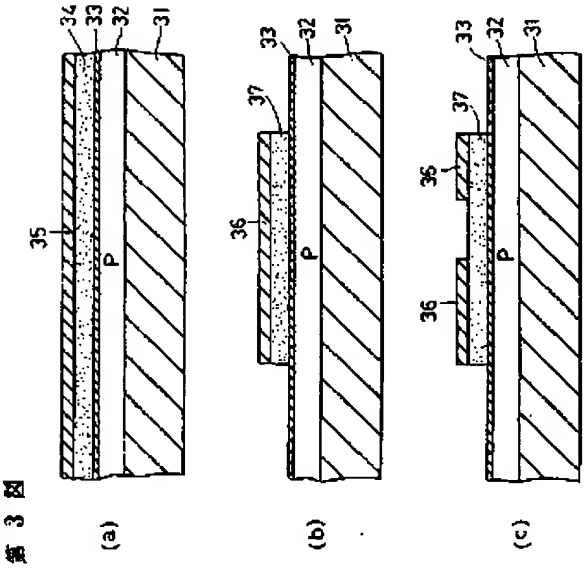
第1図



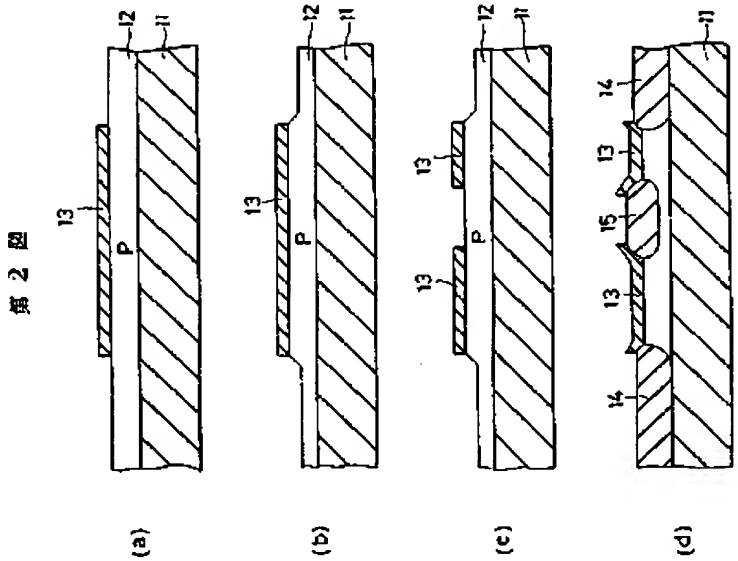
第2図



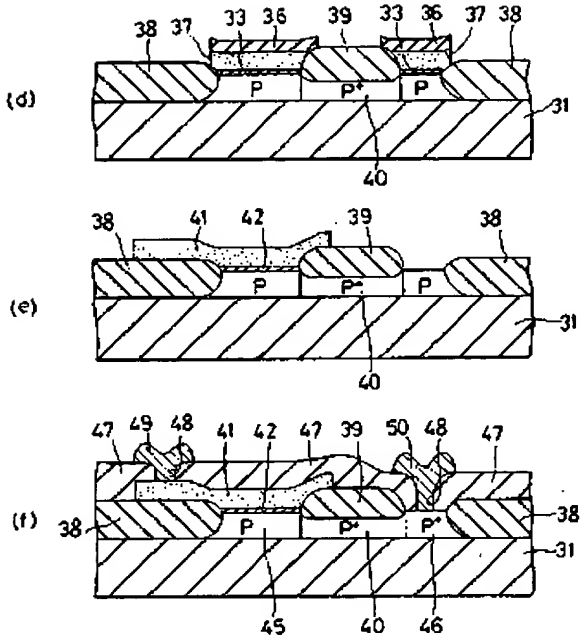
第3図



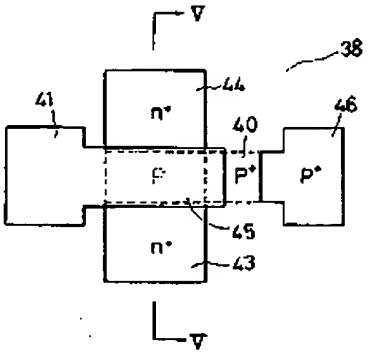
第2図



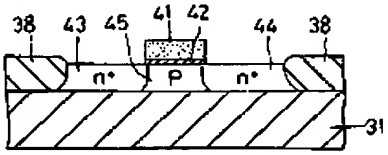
第 3 図



第 4 図



第 5 図



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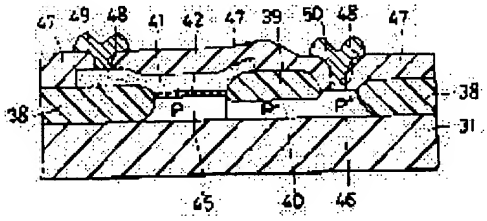
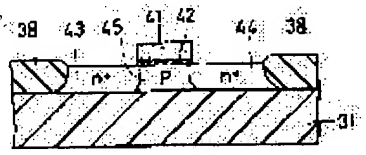
(71)Applicant : **TOSHIBA CORP**
(72)Inventor : **MATSUMURA HOMARE**
MAEGUCHI KENJI

(54) MANUFACTURE OF SEMICONDUCTOR DEVICE

(57)Abstract:
PURPOSE: To improve the circuit characteristics of a semiconductor device by forming the second oxidized film which reaches an insulating substrate on the region exposed with silicon pattern and the third oxidized film which reaches at least the first oxidized film and does not reach the substrate, thereby eliminating the floating state of the substrate while corresponding to the trend to the decrease in the thickness of a silicon layer.
CONSTITUTION: Though the thickness of a silicon layer formed on a sapphire substrate 31 is extremely thin, e.g., 4,000Å, a p+ type impurity layer 40 having sufficient thickness to become wirings between the third oxidized film 39 and the substrate 31 can remain. Accordingly, a semiconductor base 45 between a source region 43 and a drain region 44 can be externally led through the layer 40 and the base leading region 46, and the potential can be fixed. Thus, the circuit characteristics can be improved. Further, since the third oxidized film 39 on the layer 40 to become wirings is thick, the floating capacity between the wirings and the silicon layer can be reduced, and the circuit characteristics such as propagation velocity and the like does not deteriorate.





LEGAL STATUS

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INVENTOR-INFORMATION:
NAME
MATSUMURA, HOMARE
MAEGUCHI, KENJI

ASSIGNEE-INFORMATION:
NAME COUNTRY
TOSHIBA CORP N/A

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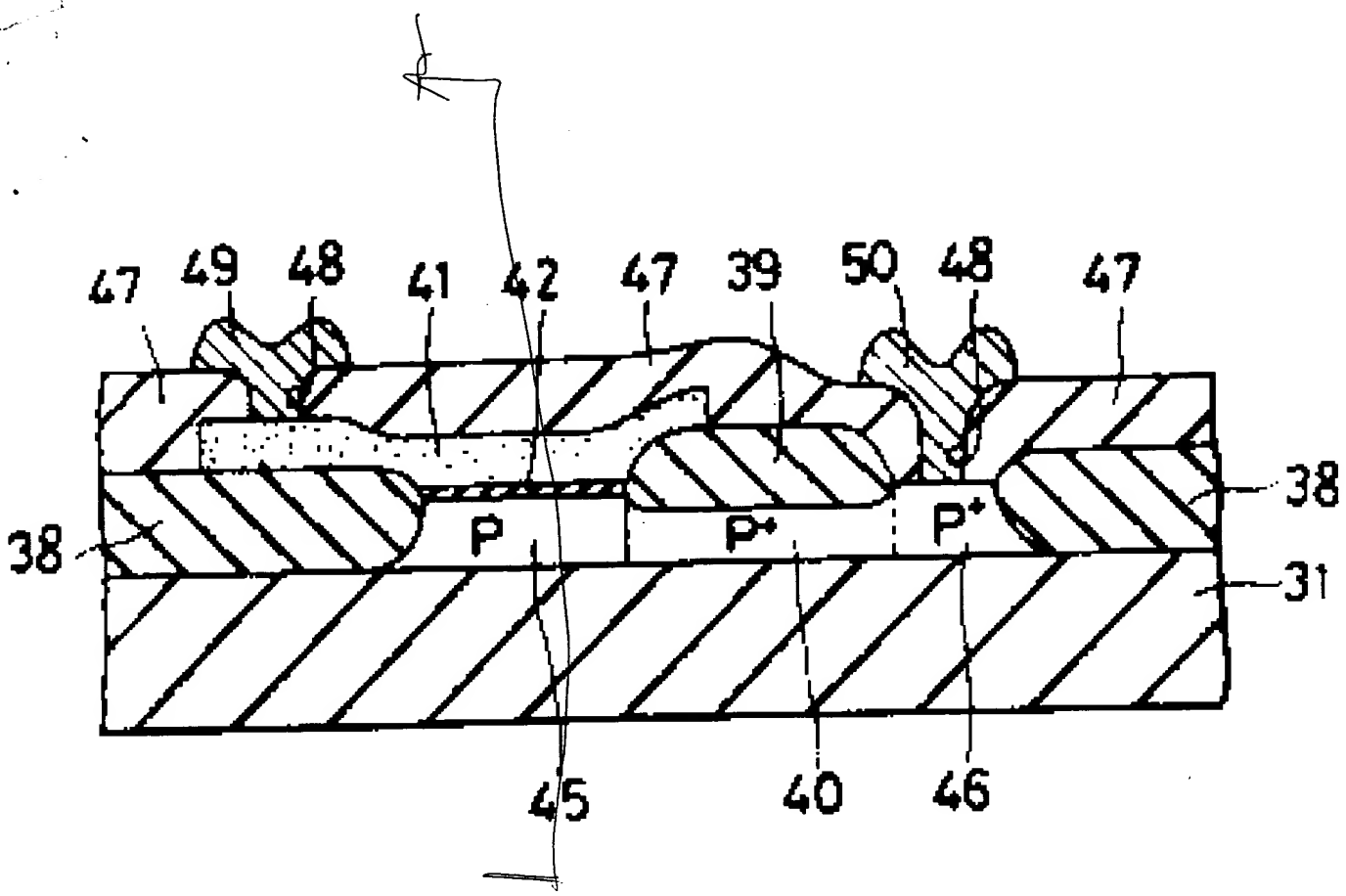
US-CL-CURRENT: 438/158,438/479 ,438/FOR.244

ABSTRACT:

PURPOSE: To improve the circuit characteristics of a semiconductor device by forming the second oxidized film which reaches an insulating substrate on the region exposed with silicon pattern and the third oxidized film which reaches at least the first oxidized film and does not reach the substrate, thereby eliminating the floating state of the substrate while corresponding to the trend to the decrease in the thickness of a silicon layer.

CONSTITUTION: Though the thickness of a silicon layer formed on a sapphire substrate 31 is extremely thin, e.g., 4,000Å, a p<SP>+</SP> type impurity layer 40 having sufficient thickness to become wirings between the third oxidized film 39 and the substrate 31 can remain. Accordingly, a semiconductor base 45 between a source region 43 and a drain region 44 can be externally led

through the layer 40 and the base leading region 46, and the potential can be fixed. Thus, the circuit characteristics can be improved. Further, since the third oxidized film 39 on the layer 40 to become wirings is thick, the floating capacity between the wirings and the silicon layer can be reduced, and the circuit characteristics such as propagation velocity and the like does not deteriorate.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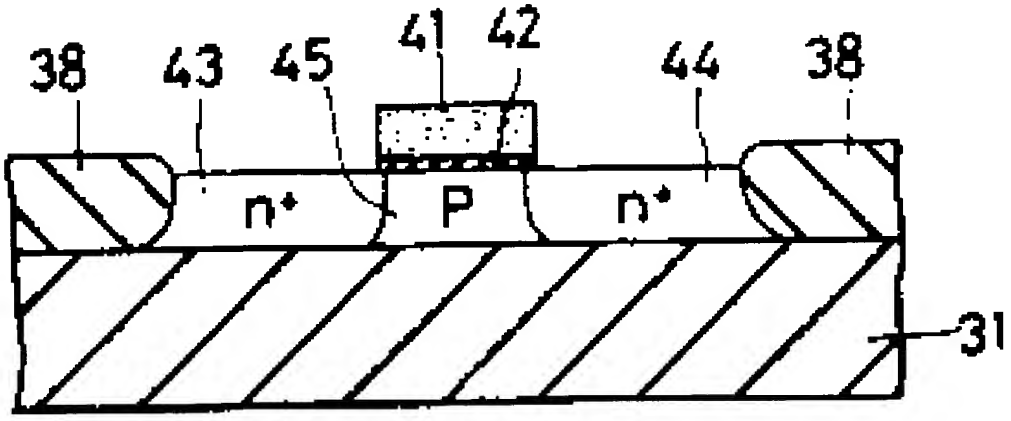
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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] Especially this invention relates to the semiconductor device which has the separation insulator layer (partialness STI (Partial Shallow Trench Isolation) is called below) which the base does not reach to an embedded oxide film, and its manufacture method about the semiconductor device and its manufacture method of SOI (Silicon On Insulator) structure.
[0002]
[Description of the Prior Art] The semiconductor device which has the SOI structure which consists of a semiconductor substrate, an embedded oxide film, and a semiconductor layer Since the active region is enclosed by an embedded oxide film and the isolation (Full STI (Full Shallow Trench Isolation) is called below) which the base reaches to an embedded oxide film, Since there is no fear of a latch rise taking place and the source drain field is in contact with the embedded oxide film, even if it forms a CMOS transistor, While a junction capacitance is small compared with the semiconductor device with which the direct transistor was formed in the semiconductor substrate front face and high-speed operation is possible, the leakage current at the time of standby also becomes small, and it has the advantage that power consumption can be suppressed. The thickness of the semiconductor layer formed on the embedded oxide-film front face 0.15 micrometers or more, for example however, in a certain case The carrier (nMOS a hole and pMOS electron) generated according to an ionization by collision phenomenon collects in the semiconductor layer of the lower part of a channel formation field. Since there are various troubles produced according to the substrate suspension effects, like the frequency dependence of a time delay comes out since a kink occurs by this, pressure-proofing of operation does not deteriorate and the potential of a channel field is not stabilized, generally the potential of a channel formation field is fixed. The semiconductor device with which the potential of a channel formation field was fixed is indicated in this way by JP,58-124,243,A.
[0003] In recent years, since potential of a channel formation field is not further fixed for every transistor, but the potential of the channel formation field of two or more transistors of the same conductivity type is fixed collectively, partialness STI separates, detailed-ization is attained and this structure is indicated by IEEE International SOI Conference, Oct.1997, etc.
[0004] Drawing 26 is the plan showing the conventional semiconductor device, and, as for a gate electrode, and 107 and 108, for 104, a separation insulator layer and 106 are [a source drain field and 109] wiring in drawing. As shown in drawing, in the case of partialness STI, the wiring 109 for fixing the potential of a channel formation field is formed to two or more transistors of the same conductivity type, and it is. Drawing 27 is the cross section showing the conventional semiconductor device, and is a cross section in the X-X cross section of drawing 26 . For an embedded oxide film and 1010, as for a gate insulator layer and 103, in drawing, a channel formation field and 105 are [101 / a semiconductor substrate and 102 / a semiconductor layer and 1011] channel cut layers. As shown in drawing, the separation insulator layer 104 between two adjoining transistors does not reach the embedded oxide film 102, but the channel cut layer 1011 containing the high-concentration impurity of the same conductivity type as the channel formation field 1010 is formed in the bottom of the separation insulator layer. 104. And two channel formation fields 1010 are in the state where it was connected through the channel cut layer 1011, and this connects with wiring 109 and is fixing the potential of the channel formation field 1010.
[0005]
[Problem(s) to be Solved by the Invention] Element separation pressure-proofing with partialness STI structure However, a low sake, To either of each wiring (not shown) linked to the source drain field of the adjoining transistor, source voltage, When the potential difference occurs between source drain fields which adjoin through a channel cut layer -- drain voltage is impressed to another side -- Since a comparatively big leakage current may have flowed in a channel cut layer, large element separation width of face had to be taken, and there was a trouble of barring detailed-ization.
[0006] Drawing 28 is the cross section showing the conventional semiconductor device, and is a cross section in the Y-Y cross section of drawing 26 . Since the separation insulator layer 104 has not reached the embedded oxide film 102 between the source drain fields of the adjoining transistor so that it may understand also from this drawing, a leakage current may flow through the channel cut layer 1011.
[0007] this invention was made in order to solve the above-mentioned technical problem, it suppresses the leakage current which flows through the channel cut layer under this separation insulator layer in the semiconductor device equipped with the separation insulator layer of the partialness STI structure which can bundle up the voltage of the channel formation field of

two or more transistors, and can be fixed, and aims at acquiring the semiconductor device which improved, and its manufacture method.

[0008]

[Means for Solving the Problem] The semiconductor device concerning this invention is equipped with the SOI substrate which serves as a semiconductor substrate and an embedded oxide film from a semiconductor layer. The separation insulator layer formed by surrounding the 1st and 2nd active regions arranged in the main front face of a semiconductor layer, and separating an embedded oxide film and a predetermined distance, The 1st active element formed in the 1st active region, and the 2nd active element formed in the 2nd active region, Since it is characterized by having the impurity layer formed in one principal plane of the semiconductor substrate near the interface with an embedded oxide film, and the wiring which connects with an impurity layer electrically and the impurity layer is formed, Pressure-proofing can be made high, while being able to suppress generating of the leakage current in this portion, even if the potential difference occurs between the transistors which adjoin through a separation insulator layer.

[0009] An impurity layer and a semiconductor layer are the 1st conductivity type. furthermore, the 1st active element It is the MOS transistor which has the 1st source field and drain field of the 2nd conductivity type which reach an embedded oxide film from the main front face of the 1st active region. the 2nd active element It is the MOS transistor which has the 2nd source field and drain field of the 2nd conductivity type which reach an embedded oxide film from the main front face of the 2nd active region. It is what is characterized by fixing the potential of an impurity layer and the semiconductor layer under a separation insulator layer. Since the voltage clamp of the impurity layer of a semiconductor substrate front face is formed and carried out by the transistor and the reverse conductivity type while fixing the potential of the semiconductor layer under a separation insulator layer, Pressure-proofing can be made high, while being able to suppress generating of the leakage current in this portion, even if the potential difference occurs between the source drain fields of the transistor which adjoins through a separation insulator layer.

[0010] An impurity layer and a semiconductor layer are the 1st conductivity type. moreover, the 1st active element It is the MOS transistor which has the 1st source field and drain field of the 2nd conductivity type which reach an embedded oxide film from the main front face of the 1st active region. the 2nd active element It is the MOS transistor which has the 2nd source field and drain field of the 2nd conductivity type which reach an embedded oxide film from the main front face of the 2nd active region. It is what is characterized by fixing the potential of an impurity layer and not fixing the potential of the semiconductor layer under a separation insulator layer. While being able to arrange mutual threshold voltage with a sufficient precision by making the channel formation field of the adjoining transistor into floating, and sharing it, without fixing the potential of the semiconductor layer under a separation insulator layer Since the voltage clamp of a transistor and the impurity layer of a reverse conductivity type is formed and carried out to the semiconductor substrate front face under a separation insulator layer, Pressure-proofing can be made high, while being able to suppress generating of the leakage current in this portion, even if the potential difference occurs between the source drain fields of the transistor which adjoins through a separation insulator layer.

[0011] A semiconductor layer is the 1st conductivity type and an impurity layer is the 2nd conductivity type. moreover, the 1st active element It is the MOS transistor which has the 1st source field and drain field of the 2nd conductivity type which were formed by separating an embedded oxide film and a predetermined distance from the main front face of the 1st active region. The 2nd active element is a MOS transistor which has the 2nd source field and drain field of the 2nd conductivity type which were formed by separating an embedded oxide film and a predetermined distance from the main front face of the 2nd active region. The voltage impressed to an impurity layer is what is characterized by being a reverse bias to a semiconductor substrate. When a reverse bias impresses this voltage to a semiconductor substrate at an impurity layer in the case of the structure which the source drain field has not attained to the embedded oxide film Pressure-proofing can be made high, while being able to suppress generating of the leakage current in this portion, even if the potential difference occurs between the source drain fields of the transistor which adjoins through a separation insulator layer.

[0012] Moreover, the voltage which reaches an embedded oxide film from the semiconductor layer front face under a separation insulator layer, adjoins mutually, and serves as a reverse bias is further equipped with the 1st impurity range of the 1st conductivity type impressed, respectively, and the 2nd impurity range of the 2nd conductivity type. The 1st active element reaches an embedded oxide film from the main front face of the 1st active region. Either is the MOS transistor which has the 1st source field and drain field of the 2nd conductivity type which adjoin the 1st impurity range. the 2nd active element It is the MOS transistor which has the 2nd source field and drain field of the 1st conductivity type where an embedded oxide film is reached from the main front face of the 2nd active region, and either adjoins the 2nd impurity range. The voltage impressed to an impurity layer is what is characterized by being a reverse bias to a semiconductor substrate. Pressure-proofing can be made high, while suppressing generating of the leakage current in this portion, even if the potential difference occurs between the source drain fields which adjoin through a separation insulator layer, since the potential of the 1st, the 2nd impurity range, and an impurity layer is fixed.

[0013] Moreover, the voltage which reaches an embedded oxide film from the semiconductor layer front face under a separation insulator layer, adjoins mutually, and serves as a reverse bias is further equipped with the 1st impurity range of the 1st conductivity type impressed, respectively, and the 2nd impurity range of the 2nd conductivity type. The 3rd impurity range of the 2nd conductivity type by which the 1st active element adjoins the 1st impurity range, It is the diode equipped with the 4th impurity range of the 1st conductivity type which adjoins this 3rd impurity range. the 2nd active element It is the

diode equipped with the 5th impurity range of the 1st conductivity type which adjoins the 2nd impurity range, and the 6th impurity range of the 2nd conductivity type which adjoins this 5th impurity range. The voltage impressed to an impurity layer is what is characterized by being a reverse bias to a semiconductor substrate. Pressure-proofing can be made high, while suppressing generating of the leakage current in this portion, even if the potential difference occurs between the impurity ranges of the reverse conductivity type of the diode which adjoins through a separation insulator layer, since the 1st, the 2nd impurity range, and an impurity layer are formed and potential is fixed.

[0014] Furthermore, since it is characterized by for an impurity layer to extend under an active region, and it is incorporated by the impurity layer and a voltage clamp is carried out to it even if the impurity poured in on the occasion of source drain field formation runs through an embedded oxide film and reaches even a semiconductor substrate by the impurity layer formed in a semiconductor substrate front face, there is no possibility may become the cause of a circuit malfunction, and the effect that the reliability of a semiconductor device improves does so.

[0015] It is what is characterized by having further functional block with which the 1st active element and the 2nd active element were formed, and different functional block. in addition, in functional block The 1st and 2nd active elements separated by partialness STI are formed in a portion with the need of fixing the potential of a channel formation field in common, according to the function needed, and the conductivity type and the voltage to impress of the impurity layer doubled with it can be determined as it.

[0016] Moreover, the process which forms an impurity layer in the semiconductor substrate front face of the SOI substrate which has the semiconductor layer formed through the embedded oxide film on the semiconductor substrate front face, The process which forms the separation insulator layer by which the 1st and 2nd active regions arranged in the main front face of a semiconductor layer are surrounded, and a part of semiconductor layer remains in the bottom of it, It can have the process which forms the 1st active element in the 1st active region, the process which forms the 2nd active element in the 2nd active region, and the process which forms wiring linked to an impurity layer, and the semiconductor device which can fix the potential of an impurity layer through wiring can be manufactured. Furthermore, since it incorporates in an impurity layer even if the impurity by which the ion implantation was carried out runs through an embedded oxide film and reaches even a semiconductor substrate in case it is impurity-range formation since an impurity layer can be formed even not only in an isolation region but in the bottom of an active region, there is no possibility of becoming the cause of a circuit malfunction, and the manufacture method of a semiconductor device which improved can be acquired.

[0017] Furthermore, the 1st active element and 2nd active element Are the MOS transistor which has the same conductivity type, and the process which forms a separation insulator layer The process which forms a wrap mask for the active-region front-face top of a semiconductor layer, and forms the slot which leaves a pars basilaris ossis occipitalis, **********s from a half-conductor-layer main front face, and encloses an active region, The process which forms an insulator layer in the whole surface, and the process which removes the insulator layer on a mask front face, It is what is characterized by having had the process which removes a mask and having further the process which carries out the ion implantation of the high-concentration impurity by the same conductivity type as a semiconductor layer into Mizoshita's semiconductor layer in front of the process which forms an insulator layer after the process which forms a slot. Since the ion implantation of the high-concentration impurity is carried out to the semiconductor layer under a separation insulator layer rather than a semiconductor layer and the channel cut layer is formed, the semiconductor device whose separation property improved further can be obtained.

[0018] Moreover, the 1st active element is the MOS transistor which has the 1st conductivity type. The process which forms the 1st mask which has opening on the separation insulator layer of the 1st active element before the process which forms the 1st active element after the process which the 2nd active element is a MOS transistor which has the 2nd conductivity type, and forms a separation insulator layer, The process which carries out the ion implantation of the impurity which has the 2nd conductivity type on the whole surface to the whole surface, and forms the 1st impurity range in the semiconductor layer under the separation insulator layer of the 1st active element, The process which removes the 1st mask, and the process which forms the 1st mask which has opening on the separation insulator layer of the 1st active element, The process which carries out the ion implantation of the impurity which has the 2nd conductivity type on the whole surface to the whole surface, forms the 1st impurity range in the semiconductor layer under the separation insulator layer of the 1st active element, and removes the 1st mask, The process which forms the 2nd mask which has opening on the separation insulator layer of the 2nd active element, It is what carries out the ion implantation of the impurity which has the 1st conductivity type on the whole surface to the whole surface, and is characterized by having the process which forms the 2nd impurity range in the semiconductor layer under the separation insulator layer of the 2nd active element, and removes the 2nd mask. One side of the source drain field of a pMOS transistor and a nMOS transistor, and the 1st formed in the bottom of a separation insulator layer and the semiconductor device arranged so that the 2nd impurity range might serve as pnpn can be obtained.

[0019] Moreover, form a wrap mask for a 1st [which was arranged in the main front face of the semiconductor layer formed through the embedded oxide film on the semiconductor substrate front face], and 2nd active-region front-faces top, and from a half-conductor-layer main front face, leave a pars basilaris ossis occipitalis and it **********s. The ion implantation of the impurity is carried out into the process which forms the slot which encloses the 1st and 2nd active regions, and Mizoshita's semiconductor substrate. The process which forms an impurity layer in the front face of a semiconductor substrate, and the process which forms an insulator layer in the whole surface, The process which removes the insulator layer on a mask front face, and the process which removes a mask, It can have the process which forms the 1st active element in the 1st active region, the process which forms the 2nd active element in the 2nd active region, and the process which forms wiring linked to

an impurity layer, and the semiconductor device which can fix the potential of an impurity layer through wiring can be manufactured.

[0020] Furthermore, the 1st active element and 2nd active element After the process which is the MOS transistor which has the same conductivity type, and forms a slot, It is what is characterized by having further the process which carries out the ion implantation of the high-concentration impurity by the same conductivity type as a semiconductor layer into Mizoshita's semiconductor layer in front of the process which forms an insulator layer. Since the ion implantation of the high-concentration impurity is carried out to the semiconductor layer under a separation insulator layer rather than a semiconductor layer and the channel cut layer is formed, the semiconductor device whose separation property improved further can be obtained.

[0021]

[Embodiments of the Invention] Gestalt 1. drawing 1 of operation is the cross section of the semiconductor device concerning the gestalt 1 of implementation of this invention, and is set to drawing 1 . In 1, a p type semiconductor substrate and 2 a semiconductor layer and 4 for an embedded oxide film and 3 A separation insulator layer, 5 a gate electrode, and 7, 8, 71 and 81 for a gate insulator layer and 6 A source drain field, 9 and 91 a channel formation field and 11 for wiring and 10 A channel cut layer, As for a sidewall, and 14 and 141, for 12, a layer insulation film, and 15 and 151 are [an impurity layer and 13] contact holes, and the source drain fields 7, 8, 71, and 81 and the channel cut layer 11 inject an impurity into the semiconductor layer 3, and are formed. The semiconductor substrate 1, the embedded oxide film 2, and the semiconductor layer 3 constitute the so-called SOI substrate, and which methods, such as a lamination method and the SIMOX method, are sufficient as the formation method.

[0022] When the thickness of the semiconductor layer 3 is [the thickness of about 30-200nm and the embedded oxide film 2] about 0.04-0.4 micrometers, The channel cut layer 11 p type impurities, such as boron, about three 1x1017 to 1x1018-/cm, As for the impurity layer 12, about three 1x1017 to 1x1019-/cm and the channel formation field 10 contain [the impurity of p types, such as boron,] about three 1x1017 to 1x1018-/cm for p type impurities, such as boron, respectively. Although concentration of the channel cut layer 11 may be made the same as the channel formation field 10, a separation property improves, so that concentration is high. Moreover, including which arsenic n type impurity about three 1x1019 to 1x1021-/cm, the source drain fields 71 and 81 are prolonged to the embedded oxide film 2, including n type impurities, such as Lynn and an arsenic, about three 1x1017 to 1x1020-/cm, and the source drain fields 7 and 8 have LDD (Lightly Doped Drain) structure. Although the gate electrode 6 is formed with contest polysilicon which contained n type impurities, such as Lynn, about three two to 15x1020-/cm, the laminated structure of the contest the polysilicon and metal silicide layers, such as WSix, which contained the impurity besides this, or metals, such as W, Mo, Cu, and aluminum, are sufficient as it. Moreover, cobalt silicide may be formed in the front face of the gate electrode 6 and the source drain fields 7 and 8 (not shown).

[0023] The active region in which one or more transistors were formed is enclosed by the fractional separation field which consists of separation insulator layers 4 formed in the semiconductor layer 3, such as the channel cut layer 11 and a silicon oxide, it dissociates mutually, and separation width of face is 200nm - about 500nm. Moreover, the thickness of the separation insulator layer 4 is set up so that the thickness of the channel cut layer 11 under it may be set to about 10-100nm. And although it is desirable on micro processing that it is the same as that of the front face of the semiconductor layer 3 as for the upper surface of the separation insulator layer 4, if it is fully going to leave the thickness of the channel cut layer 11 when the semiconductor layer 3 is thin, since it will become difficult to take thickness required for isolation, the direction of an isolation performance which formed the upper surface of the separation insulator layer 4 more highly than semiconductor layer 3 front face improves. Moreover, between the semiconductor layer 3 and the separation insulator layer 4, the about 5-30nm silicon oxide is formed if needed (not shown). Here, although the silicon oxide is used for the isolation region, other insulator layers, such as a silicon nitride, a silicon oxidization nitride, and a silicon oxidization fluoridation film (SiOF), are sufficient. As a gate insulator layer 5, there are SiO2, SiON, and SiO2/Si3N4/SiO2 (ONO) structure, Ta 2O5, aluminum2O 3, etc.

[0024] Moreover, drawing 2 is the plan of the semiconductor device concerning the gestalt 1 of implementation of this invention, and drawing 1 is a cross section in the A-A cross section shown in drawing 2 . As for 92 or 94, in drawing 2 , wiring and 111 are impurity ranges. It connected with the gate electrode 6 electrically, and wiring 92 gave the gate voltage and has connected wiring 93 to an impurity range 111 electrically. Drawing 3 is the cross section of the semiconductor device concerning the gestalt 1 of implementation of this invention, and is a cross section in the B-B cross section shown in drawing 2 . In drawing, 152 is a contact hole. With reference to drawing, voltage is impressed to an impurity range 111 through wiring 93, and the potential of the channel formation field 10 connected through the channel cut layer 11 is fixed to it. The impurity range 111 contains the impurity of the same conductivity type as the channel formation field 10, and although it may be of the same grade as a channel formation field about the high impurity concentration, further high concentration can hold down to low resistance.

[0025] Moreover, drawing 4 is the cross section of the semiconductor device concerning the gestalt 1 of implementation of this invention, and is a cross section in the C-C cross section shown in drawing 2 . In drawing, 95 is wiring and 153 and 154 are contact holes. With reference to drawing, wiring 94 embeds the inside of the contact hole 153 formed in the layer insulation films 14 and 141, is formed, connects to the impurity layer 12 the inside of the semiconductor layer 3 and the contact hole 154 formed in the embedded oxide film 2 through the wiring 95 embedded and formed, and is fixing the potential of the impurity layer 12. Since the impurity layer 12 and the channel formation field 10 are controlled by each, the separation

insulator layer 4 which encloses the circumference of the semiconductor layer 3 in which the contact hole 154 for this wiring 95 being formed is formed is Full STI altogether, and the semiconductor layer 3 in which the element was formed is separated completely.

[0026] Drawing 5 is a graph which shows a concentration distribution of the impurity contained in the semiconductor device concerning the gestalt 1 of implementation of this invention, and shows the concentration distribution of the impurity contained in the semiconductor layer 3, the embedded oxide film 2, and the semiconductor substrate 1 in the D-D cross section shown in drawing 1 . In order to carry out the segregation of the boron poured in in order to form the impurity layer 12 to a front face with heat treatment of various processes, it has the distribution as shown in drawing.

[0027] Next, operation is explained. In the case of a nMOS transistor, with reference to drawing 1 , the voltage impressed to each electrode It is VG=0-1.8V, VD=0-1.8V, VS=0V, and about VB=0--1V. A channel is formed in channel formation field 10 front face under the gate electrode 5, either the source drain fields 7 and 71 or the source drain fields 8 and 81 turn into a source field, another side turns into a drain field, and it operates as a circuit. At this time, 1V or -1V are impressed to 0V and the impurity layer 12 in the channel formation field 10, respectively. Such voltage is examples and is changed by gate insulation thickness or gate length. Moreover, if the absolute value of the voltage which will be impressed to the impurity layer 12 if the thickness of the embedded oxide film 2 becomes thick becomes large and the thickness of the embedded oxide film 2 becomes thin, the absolute value of the voltage impressed to the impurity layer 12 will become small.

[0028] Drawing 6 is a graph which shows the leakage current of the semiconductor device concerning the gestalt 1 of implementation of this invention, in the semiconductor device shown in drawing 1 , sets width of face of 40nm and the separation insulator layer 4 to 0.2 micrometers for the thickness of 0.15 micrometers and the embedded oxide film 2, and carries out the simulation of the thickness of the semiconductor layer 3. In this graph, the leakage current which generated the source drain fields 7 and 71 of the transistor which adjoins through the separation insulator layer 4, and the potential difference generated between 8 and 81 in a horizontal axis and during this period is taken along a vertical axis. Among drawing, when, as for O, the impurity layer 12 is not formed and ** impresses -1V to the impurity layer 12, ** expresses with the impurity layer 12 the case where 1V are impressed, respectively. This drawing shows that a leakage current decreases and pressure-proofing is also improving by forming the impurity layer 12.

[0029] In the gestalt of this operation, although drawing where the impurity layer 12 was formed in the whole surface explained, if the impurity layer 12 is formed only in the lower part of the portion for which partialness STI is used as isolation, it can raise a separation property. Moreover, although an example of the portion which a nMOS transistor adjoins was explained, also by the portion which a pMOS transistor adjoins, it is the same and all can be applied to the portion to which the potential difference is born by circuit arrangement here in the portion which the source drain fields 7 and 71 of the same conductivity type, and 8 and 81 adjoin through partialness STI. In the case of a pMOS transistor, although the voltage which the conductivity type of each impurity range except the semiconductor substrate 1 becomes reverse, and impresses also becomes **1V at 1.8V and the impurity layer 12 VG=0-1.8V, VD=0-1.8V, VS=1.8V, about VB=1.8V, and in the channel formation field 10, respectively, also in an n type case, it is about the impurity contained in contest polysilicon of the gate electrode 6. Furthermore, in the gestalt of this operation, although explained using the semiconductor device with which the number of layers of the layer insulation film formed between transistors differs from arrangement etc., and one transistor was formed in one active region of the composition of a circuit although an example about wiring 9 and arrangement of 91-94 was shown, it is not restricted to especially this.

[0030] According to this semiconductor device, two or more transistors which are formed on an embedded oxide film and have the same conductivity type on the semiconductor substrate front face under the separation insulator layer 4 of the partialness STI structure separated mutually Since the voltage clamp of a transistor and the impurity layer of a reverse conductivity type is formed and carried out, Even if the potential difference occurs between the source drain fields of the transistor which adjoins through a separation insulator layer, while being able to suppress generating of the leakage current in this portion, pressure-proofing can be made high, and even if it turns minutely, the semiconductor device whose separation property improved can be obtained. Moreover, since it is incorporated by the impurity layer 12 and potential is being fixed even if the impurity poured in on the occasion of source drain field formation runs through an embedded oxide film 2 and reaches even a semiconductor substrate 1 when an impurity layer 12 is prolonged and formed not only in the bottom of a separation insulator layer but in the bottom of a source drain field 71 and 81, there is no possibility of may become the cause of a circuit malfunction, and the effect that the reliability of a semiconductor device improves does so.

[0031] Moreover, since high sensitivity is required, the transistor used as a sense amplifier (cross-linking type amplifier) etc. can arrange mutual threshold voltage with a sufficient precision by making the channel formation field of the adjoining transistor into floating, and sharing it. In such a case, in order to make it not influenced of other transistors, only separation between transistors to share is set to partialness STI, and separation with other portions is taken as Full STI. Therefore, the cross section of the portion which makes a channel formation field floating is the same as that of what was shown in drawing 1 . Drawing 7 is a graph which shows the leakage current of the semiconductor device concerning the gestalt 1 of implementation of this invention, in the semiconductor device shown in drawing 1 , sets width of face of 40nm and the separation insulator layer 4 to 0.2 micrometers for the thickness of 0.15 micrometers and the embedded oxide film 2, and carries out the simulation of the thickness of the semiconductor layer 3, and voltage is not impressed to the channel formation field 10, namely, the body is in the state of floating. In this graph, the leakage current which generated the source drain fields 7 and 71 of the transistor which adjoins through the separation insulator layer 4, and the potential difference generated

between 8 and 81 in a horizontal axis and during this period is taken along a vertical axis. Among drawing, when, as for O, the impurity layer 12 is not formed, ** expresses with the impurity layer 12 the case where 1V are impressed, respectively. By forming the impurity layer 12 and impressing 1V from this drawing, shows that pressure-proofing is improving. Although the sense amplifier is raised as an example which makes a channel formation field floating here, even if it is the transistor used as a sense amplifier, it cannot be overemphasized that the potential of a channel formation field may be fixed.

[0032] Here, although an example of the portion which a nMOS transistor adjoins was explained, also by the portion which a pMOS transistor adjoins, it is the same and all can be applied to the portion to which the potential difference is born by circuit arrangement in the portion which the source drain fields 7 and 71 of the same conductivity type, and 8 and 81 adjoin through partialness STI. In the case of a pMOS transistor, the conductivity type of each impurity range becomes reverse, the voltage to impress also becomes VG=0-1.8V, VD=0-1.8V, VS=1.8V, about VB=1.8V, and the impurity layer 12 with -1V, respectively, and it does not need to be formed by wiring 93 and the impurity range 111, either.

[0033] In the semiconductor device with which voltage is impressed as described above By being formed on an embedded oxide film, making into floating the channel formation field of the transistor which adjoins through the separation insulator layer of partialness STI structure which separates two or more transistors of each other which have the same conductivity type, and sharing it Since the voltage clamp of a transistor and the impurity layer of a reverse conductivity type is formed and carried out to the semiconductor substrate front face under a separation insulator layer while being able to arrange mutual threshold voltage with a sufficient precision, Even if the potential difference occurs between the source drain fields of the transistor which adjoins through a separation insulator layer, while being able to suppress generating of the leakage current in this portion, pressure-proofing can be made high, and even if it turns minutely, the semiconductor device whose separation property improved can be obtained.

[0034] Next, the manufacture method of the semiconductor device concerning the gestalt 1 of implementation of this invention is explained. Drawing 8 - drawing 13 are the cross sections showing one process of the manufacture method of a semiconductor device which shows the gestalt 1 of operation. In nMOS, the impurity of p types, such as boron, and in pMOS, with reference to drawing, the ion implantation of the impurity of n types, such as Lynn, is carried out from on the front face of the SOI substrate equipped with the embedded oxide film 2 and the semiconductor layer 3 on the front face of the semiconductor substrate 1, and the impurity layer 12 is formed in the portion to which the semiconductor substrate 1 touches the embedded oxide film 2. Drawing 8 is the cross section showing the semiconductor device of the stage which this process finished. The pouring conditions at this time change with thickness of the embedded oxide film 2, and p type impurities, such as boron, are 500-600keV and about two 1x1013 to 1x1014-/cm, when embedded oxidization thickness is about 0.04 micrometers and 200-300keV, about two 1x1013 to 1x1014-/cm, and embedded oxidization thickness are about 0.4 micrometers. Moreover, the pouring conditions of n type impurities, such as Lynn, are 500-600keV and about two 1x1013 to 1x1014-/cm, when embedded oxidization thickness is about 0.04 micrometers and 200-300keV, about two 1x1012 to 1x1014-/cm, and embedded oxidization thickness are about 0.4 micrometers. Not only ion-implantation but the plasma doping method, the cluster ion beam method, etc. may be used for formation of the impurity layer 12.

[0035] As for a silicon oxide and 32, in drawing 9 , 31 is [a silicon nitride and 41] slots. With reference to drawing, the silicon oxide 31 which has about 5-30nm thickness, and the silicon nitride 32 which has about 100-300nm thickness are formed on the front face of the semiconductor layer 3, and anisotropic etching removes alternatively the silicon nitride 32 and silicon oxide 31 on an isolation region using a photoresist mask (not shown). And after removing a photoresist mask, anisotropic etching of the semiconductor substrate 1 is carried out by using the silicon nitride 32 as a mask, and the slot 41 with a depth of about 100-500nm is formed in the front face of the semiconductor substrate 1. The width of face of this slot is about 100-500nm. Then, in p type impurities, such as boron, and pMOS, in nMOS, the ion implantation of Lynn or which arsenic n type impurity is carried out to the whole surface in 10-20KeV and about two 5x1012 to 1x1013-/cm, and it forms the channel cut layer 11. Drawing 9 is the cross section showing the element of the semiconductor device in the stage which this process finished.

[0036] What is necessary is just to carry out in the stage where the slot 41 was formed, like formation of the channel cut layer 11, when forming the impurity layer 12 only in an isolation region. The pouring conditions at this time change with thickness of the embedded oxide film 2, and p type impurities, such as boron, are 450-550keV and about two 1x1013 to 1x1014-/cm, when embedded oxidization thickness is about 0.04 micrometers and 150-200keV, about two 1x1013 to 1x1014-/cm, and embedded oxidization thickness are about 0.4 micrometers. Moreover, the pouring conditions of n type impurities, such as Lynn, are 450-550keV and about two 1x1013 to 1x1014-/cm, when embedded oxidization thickness is about 0.04 micrometers and 150-250keV, about two 1x1012 to 1x1014-/cm, and embedded oxidization thickness are about 0.4 micrometers.

[0037] Next, after forming a silicon oxide in the whole surface by 300nm - about 800nm thickness by reduced pressure CVD (not shown), by the CMP (Chemical Mechanical Polishing) method which used the silicon nitride 32 as the stopper, the silicon oxide on silicon nitride 32 front face is removed, and it leaves a silicon oxide only to the interior of opening which consists of a slot 2 and a silicon nitride 32. Then, after removing the silicon nitride 32 by the wet etching by the heat phosphoric acid, a silicon oxide 31 is removed and the separation insulator layer 4 is formed. Drawing 10 is a cross section in the stage which this process finished. About the channel cut layer 11 or the impurity layer 12, in this stage, an ion implantation may be carried out and you may form. Drawing 11 is a graph which shows a concentration distribution of the impurity contained in the element of the semiconductor device in this stage, and shows the impurity atom concentration

profile in the E-E cross section shown in drawing 10 . When the separation insulator layer 4 is formed by the silicon oxide by performing a biscuit ware process at about 800-1100 degrees C, while being able to make membraneous quality precise, in this stage, the high impurity concentration of impurity layer 12 front face can go up, and resistance can be lowered in it. Drawing 12 is a graph which shows a concentration distribution of the impurity contained in the element of the semiconductor device in this stage, and shows the impurity atom concentration profile in the E-E cross section shown in drawing 10 . And after forming the silicon oxide by thermal oxidation in the whole surface (not shown), in nMOS, in boron, fluoridation boron, and pMOS, the ion implantation of Lynn or which arsenic impurity is carried out to the whole surface in 10-20KeV and about two 1x1012 to 5x1012-/cm, and it introduces the impurity which adjusts a threshold to the channel formation field 10 (not shown). A silicon oxide is for protecting a semiconductor substrate front face, and is removed from the damage in the case of an ion implantation after an ion implantation.

[0038] Next, as a gate insulator layer 5, after forming a silicon oxide in the whole semiconductor substrate 1 front face by thermal oxidation by about 7-10nm thickness, and forming about 150-300nm of polysilicon contest layers used as the gate electrode 6 in the whole surface by CVD, the polysilicon contest layer 6 used as a gate electrode is formed by carrying out patterning by the anisotropic etching using the photoresist mask (not shown). And using a photoresist mask, in nMOS, in Lynn, an arsenic, and pMOS, the ion implantation of boron, the fluoride boron, etc. is carried out, respectively in 20-40keV and about two 1x1013 to 5x1014-/cm, and the source drain fields 71 and 81 are formed. Drawing 13 is the cross section showing the element of the semiconductor device in the stage which this process finished.

[0039] Next, after depositing a silicon oxide on the whole surface in about 30-100nm thickness by CVD and forming a sidewall 13 by carrying out etchback, in nMOS, in pMOS, an arsenic etc. carries out the ion implantation of boron, the fluoridation boron, etc. in 10KeV(s) and about two one to 5x1015-/cm, and the source drain fields 7 and 8 are formed for it. Since a source drain field is made into LDD structure if needed, it may not form the source drain fields 7 and 8 by the case. The poured-in impurity is activated by annealing about 10 to 30 minutes at about 800-900 degrees C. Moreover, the rate of activation can be gathered, suppressing diffusion of an impurity, if 1050 degrees C and RTA (Rapid Thermal Anneal) processing for about 5 - 10 seconds are performed. After forming a silicon oxide by RTO (Rapid Thermal Oxidation) in that case, by CVD, the cascade screen of a silicon oxide and a silicon nitride is sufficient, it deposits, and etchback of the silicon nitride is carried out and a sidewall 13 forms it. When forming a metal silicide layer in the gate electrode 6, or the source drain field 7 and eight front faces, if it is this stage, and cobalt is deposited on the whole surface and RTA processing is carried out, it will react in the portion which silicon exposed and a metal silicide layer will be formed. Then, the cobalt which remained while it had been unreacted is removed (not shown).

[0040] And after depositing 200nm - about 600nm of silicon oxides used as the layer insulation film 14 by reduced pressure CVD, opening of the contact hole 15 which arrives at the source drain fields 7 and 71 is carried out with the diameter of 0.1 micrometers - 0.5 micrometer by the dry etching method, after embedding a wiring material by CVD to the interior, patterning is carried out, and wiring 9 is formed. Similarly, the layer insulation film 141 is formed and the contact hole 151 and wiring 91 which arrive at the source drain fields 8 and 81 are formed. Thus, the semiconductor device shown in drawing 1 is formed.

[0041] Although not illustrated here, the contact hole 152 and wiring 93 which were shown in drawing 3 , and the contact hole 153 and wiring 94 which were shown in drawing 4 are also formed similarly. Moreover, about formation sequence, although the contact hole 154 and wiring 95 which were shown in drawing 4 are also formed similarly, after forming the gate electrode 6 after forming simultaneously [after forming the layer insulation films 14 and 141] with a contact hole 153 and wiring 94 and forming the separation insulator layer 4, forming in various stages is possible. Furthermore, formation of each contact hole and wiring may be performed at another process if needed, and the formation sequence can also be changed if needed. Furthermore, a different layer insulation film and different wiring are formed in the upper layer, and may turn into a multilayer interconnection. Although there is a polysilicon contest metallurgy group into which the impurity was introduced as a wiring material, when a metal is used, it prevents that form barrier metal, such as TiN, in the wall of each contact hole, and a metal is spread to the semiconductor layer 3.

[0042] Since the impurity layer 12 can be formed in semiconductor substrate 1 front face of the semiconductor device of the SOI structure which consists of the semiconductor substrate 1, an embedded oxide film 2, and a semiconductor layer 3 according to the manufacture method of the semiconductor device shown in the gestalt 1 of this operation, Even if the potential difference occurs between the source drain fields of the transistor which has the same conductivity type formed in semiconductor layer 3 front face through the separation insulator layer of partialness STI structure by fixing the potential of this impurity layer 12 While being able to suppress generating of the leakage current in this portion, pressure-proofing can be made high, and even if it turns minutely, the manufacture method of the semiconductor device whose separation property improved can be acquired. Moreover, even if the impurity by which the ion implantation was carried out runs through the embedded oxide film 2 and reaches even the semiconductor substrate 1 in case it is source drain field formation since the impurity layer 12 can be formed even not only in an isolation region but in the bottom of an active region, it incorporates in the impurity layer 12, there is no possibility of becoming the cause of a circuit malfunction, and the manufacture method of a semiconductor device which improved can be acquired.

[0043] Gestalt 2. drawing 14 of operation is the cross section of the semiconductor device concerning the gestalt 2 of implementation of this invention, and is a cross section in the A-A cross section shown in drawing 2 . In drawing, 121 is an impurity layer. With reference to drawing, the source drain fields 71 and 81 do not reach the embedded oxide film 2, but the impurity layer 121 is formed with the impurity of the same conductivity type as a source drain field. That is, when the nMOS

transistor is adjoined and formed in semiconductor layer 3 front face, and, as for the impurity layer 121, a pMOS transistor adjoins, including the impurity of n types, such as Lynn, about two 1x1017 to 1x1020-/cm and it is formed, the impurity layer 121 contains the impurity of p types, such as boron, about three 1x1017 to 1x1020-/cm. About thickness other than this, and high impurity concentration and an impurity kind, it is the same as that of the semiconductor device shown in the gestalt 1 of operation. In the gestalt of this operation, since the area for a joint of the source drain fields 71 and 81 and the channel formation field 10 increases as compared with the gestalt 1 of operation, although a junction capacitance will increase, since the area of the plane of composition of the channel formation field 10 and the channel cut layer 11 increases, the voltage clamp of the channel formation field 10 has the advantage of becoming more certain.

[0044] Next, operation is explained. The voltage which is impressed to each electrode with reference to drawing 14 in the case of a nMOS transistor is VG=0-1.8V, VD=0-1.8V, and about VS=0V, a channel is formed in channel formation field 10 front face under the gate electrode 5, either the source drain fields 7 and 71 or the source drain fields 8 and 81 turn into a source field, another side turns into a drain field, and it operates as a circuit. The reverse biases of the voltage VB which 0V are impressed to the channel formation field 10, and is impressed to the semiconductor substrate 1 at this time should just be these conditions between the impurity layer 121 and the semiconductor substrate 1. Such voltage is examples and is changed by gate insulation thickness or gate length.

[0045] Drawing 15 is a graph which shows the leakage current of the semiconductor device concerning the gestalt 2 of implementation of this invention, in the semiconductor device shown in drawing 14 , sets width of face of 40nm and the separation insulator layer 4 to 0.2 micrometers for the thickness of 0.15 micrometers and the embedded oxide film 2, and carries out the simulation of the thickness of the semiconductor layer 3. In this graph, the leakage current which generated the source drain fields 7 and 71 of the transistor which adjoins through the separation insulator layer 4, and the potential difference generated between 8 and 81 in a horizontal axis and during this period is taken along a vertical axis. Among drawing, when, as for O, the impurity layer 121 is not formed and ** impresses -1V to the impurity layer 121, ** expresses with the impurity layer 121 the case where 1V are impressed, respectively. From this drawing, by forming the impurity layer 121 shows that the leakage current is decreasing remarkably.

[0046] In the gestalt of this operation, although drawing where the impurity layer 121 was formed in the whole surface explained, if the impurity layer 121 is formed only in the lower part of the portion for which partialness STI is used as isolation, it can raise a separation property. Furthermore, arrangement of wiring, the number of layers of the layer insulation film formed between transistors, the number of the transistor formed in one active region, etc. are examples, and are not restricted to this.

[0047] Moreover, drawing 16 is a graph which shows the leakage current of the semiconductor device concerning the gestalt 2 of implementation of this invention, and shows the leakage current in the portion which a pMOS transistor adjoins. Also in pMOS, it is the same as that of the case of nMOS, and all can be applied to the portion to which the potential difference is born by the portion which the p type source drain fields 7 and 71, and 8 and 81 adjoin through partialness STI by circuit arrangement. Although the voltage which it becomes the case where the conductivity type of each impurity range except the semiconductor substrate 1 is nMOS, and reverse in the case of a pMOS transistor, and is impressed also becomes about 1.8V in VG=0-1.8V, VD=0-1.8V, VS=1.8V, and the channel formation field 10, respectively, also in an n type case, it is about the impurity contained in contest polysilicon of the gate electrode 6. Here, in the semiconductor device shown in drawing 14 , the simulation of the thickness of the semiconductor layer 3 is carried out, using width of face of 40nm and the separation insulator layer 4 as 0.2 micrometers for the thickness of 0.15 micrometers and the embedded oxide film 2. In this graph, the leakage current which generated the source drain fields 7 and 71 of the transistor which adjoins through the separation insulator layer 4, and the potential difference generated between 8 and 81 in a horizontal axis and during this period is taken along a vertical axis. Among drawing, when, as for O, the impurity layer 121 is not formed and ** impresses 0.3V to the impurity layer 121, ** expresses with the impurity layer 121 the case where -0.3V are impressed, respectively. This drawing shows that a leakage current decreases remarkably and pressure-proofing's is improving by forming the impurity layer 121.

[0048] In the structure where the source drain field of two or more transistors which according to the semiconductor device concerning the gestalt 2 of this operation are formed on an embedded oxide film and have the same conductivity type has not reached to an embedded oxide film Since the voltage clamp of the impurity layer of the same conductivity type as a transistor is formed and carried out to the semiconductor substrate front face under the separation insulator layer of the partialness STI structure of separating the transistor of each other, Even if the potential difference occurs between the source drain fields of the transistor which adjoins through a separation insulator layer, while being able to suppress generating of the leakage current in this portion, pressure-proofing can be made high, and even if it turns minutely, the semiconductor device whose separation property improved can be obtained. Since the electric field between the source drain fields 71 and 81 and the semiconductor layer 3 under it are eased by furthermore impressing voltage to the impurity layer 121, the leakage current by BTBT (Band to Band Tunneling), the trap reed SUTEDDODONNE ring (Trap Assisted Tunneling:TAT), SRH (Shockley-Read-Hall) process, impact ionization, etc. can decrease, and power consumption can be reduced. Moreover, since it will be incorporated by the impurity layer 121 even if the impurity poured in on the occasion of source drain field formation runs through an embedded oxide film 2 and reaches even a semiconductor substrate 1 when an impurity layer 121 is prolonged and formed not only in the bottom of a separation insulator layer but in the bottom of the source drain field 71 and 81, there is no possibility may become the cause of a circuit malfunction, and the effect that the reliability of a semiconductor device improves does so.

[0049] Moreover, in the case of the transistor used as a sense amplifier (cross-linking type amplifier) etc., like the gestalt 1 of operation, the channel formation field of the adjoining transistor may be made into floating, and may be shared. Drawing 17 is a graph which shows the leakage current of the semiconductor device concerning the gestalt 2 of implementation of this invention, when the nMOS transistor adjoins in the semiconductor device shown in drawing 14 , in the thickness of 0.15 micrometers and the embedded oxide film 2, it carries out a simulation, using thickness of the semiconductor layer 3 as 0.2 micrometers, and voltage is not impressed [thickness / width of face / of 40nm and the separation insulator layer 4] to the channel formation field 10. In this graph, the leakage current which generated the source drain fields 7 and 71 of the transistor which adjoins through the separation insulator layer 4, and the potential difference generated between 8 and 81 in a horizontal axis and during this period is taken along a vertical axis. Among drawing, when, as for O, the impurity layer 121 is not formed and ** impresses 1V to the impurity layer 121, ** expresses with the impurity layer 121 the case where -1V are impressed, respectively. By impressing the voltage which forms the impurity layer 121 and becomes a semiconductor substrate and a reverse bias from this drawing shows that a leakage current decreases remarkably and pressure-proofing's is improving.
[0050] As described above, with the structure where the source drain field of the transistor which adjoins through the separation insulator layer of partialness STI structure which separates two or more transistors of each other which are formed on an embedded oxide film and have the same conductivity type has not reached to an embedded oxide film While being able to arrange mutual threshold voltage with a sufficient precision by making a channel formation field into floating and sharing it Since the voltage clamp of the impurity layer of the same conductivity type as a transistor is formed and carried out to the semiconductor substrate front face under a separation insulator layer, Even if the potential difference occurs between the source drain fields of the transistor which adjoins through a separation insulator layer, while being able to suppress generating of the leakage current in this portion, pressure-proofing can be made high, and even if it turns minutely, the semiconductor device whose separation property improved can be obtained.
[0051] Next, the manufacture method of the semiconductor device concerning the gestalt 2 of implementation of this invention is explained. Drawing 18 is the cross section showing one process of the manufacture method of the semiconductor device concerning the gestalt 2 of implementation of this invention. First, when forming nMOS and forming the impurity of n types, such as Lynn, and pMOS from on the front face of the SOI substrate equipped with the embedded oxide film 2 and the semiconductor layer 3 on the front face of the semiconductor substrate 1, the impurity of p types, such as boron, is poured in, and the impurity layer 121 is formed in the portion to which the semiconductor substrate 1 touches the embedded oxide film 2. Drawing 18 is the cross section showing the semiconductor device of the stage which this process finished. The pouring conditions at this time change with thickness of the embedded oxide film 2, and p type impurities, such as boron, are 500-600keV and about two 1x1013 to 1x1014-/cm, when embedded oxidization thickness is about 0.04 micrometers and 200-300keV, about two 1x1013 to 1x1014-/cm, and embedded oxidization thickness are about 0.4 micrometers. Moreover, the pouring conditions of n type impurities, such as Lynn, are 500-600keV and about two 1x1013 to 1x1014-/cm, when embedded oxidization thickness is about 0.04 micrometers and 200-300keV, about two 1x1012 to 1x1014-/cm, and embedded oxidization thickness are about 0.4 micrometers.
[0052] Next, like the gestalt 1 of operation, the channel cut layer 11 and the separation insulator layer 4 are formed, and the impurity (not shown) which adjusts a threshold to the channel formation field 10 is introduced. And like the gestalt 1 of operation, after forming the gate insulator layer 5 and the gate electrode 6, in nMOS, in Lynn, an arsenic, and pMOS, the ion implantation of boron, the fluoride boron, etc. is carried out, respectively in 10-30keV and about two 1x1013 to 5x1014-/cm, and the source drain fields 71 and 81 are formed if needed. when forming the impurity range (a pocket layer -- not shown) of the reverse conductivity type which furthermore encloses a source drain field, in nMOS, in boron and pMOS, the ion implantation of the impurities, such as Lynn, is carried out here in 10KeV(s) and about two 1x1012 to 1x1013-/cm (not shown) Then, after forming a sidewall 13, in nMOS, in pMOS, an arsenic etc. carries out the ion implantation of boron, the fluoridation boron, etc. in 10KeV(s) and about two one to 5x1015-/cm, and the source drain fields 7 and 8 are formed for it. And the layer insulation films 14 and 141, a contact hole 15 and 151-154, wiring 9, and 91-95 are formed like the gestalt 1 of operation.
[0053] According to the manufacture method of the semiconductor device shown in the gestalt 2 of this operation, the impurity layer 121 can be formed in semiconductor substrate 1 front face of the semiconductor device of the SOI structure which consists of the semiconductor substrate 1, an embedded oxide film 2, and a semiconductor layer 3. Since the transistor which has the source drain field of the same conductivity type as the impurity layer 121 can furthermore be formed in the front face of the semiconductor layer 3 Even if the potential difference occurs between the source drain fields of the transistor which adjoins through the separation insulator layer of partialness STI structure by fixing the potential of this impurity layer 121 While being able to suppress generating of the leakage current in this portion, pressure-proofing can be made high, and even if it turns minutely, the manufacture method of the semiconductor device whose separation property improved can be acquired. Moreover, even if the impurity by which the ion implantation was carried out runs through the embedded oxide film 2 and reaches even the semiconductor substrate 1 in case it is source drain field formation since the impurity layer 121 can be formed even not only in an isolation region but in the bottom of an active region, it incorporates in the impurity layer 121, there is no possibility of becoming the cause of a circuit malfunction, and the manufacture method of a semiconductor device which improved can be acquired.
[0054] Gestalt 3. drawing 19 of operation is the cross section of the semiconductor device in which the gestalt 3 of implementation of this invention is shown, and, as for a channel formation field, and 113 and 114, for 72-75, and 82-85, a

source drain field, and 120 and 130 are [a channel cut layer and 122] impurity layers in drawing. The gestalt of this operation shows the case where one side of the transistor which adjoins through the separation insulator layer 4 (partialness STI) is nMOS, and another side is pMOS. Moreover, when embedded oxidization thickness is 0.04 micrometers - about 0.4 micrometers, the thickness of the impurity layer 122 is the same as that of the gestalten 1 and 2 of operation. n type impurities, such as Lynn, are included about three 5x1017 to 1x1020-/cm. As for the channel cut layer 113, the channel cut layer 114 contains p type impurities, such as boron, about three 1x1017 to 1x1018-/cm, including n type impurities, such as Lynn, about three 1x1017 to 1x1020-/cm. Moreover, as for the channel formation field 120, the channel formation field 130 contains p type impurities, such as boron, about three 5x1017 to 1x1018-/cm, including n type impurities, such as Lynn, about three 5x1017 to 2x1018-/cm. The source drain field and the gate electrode are the same as that of the gestalt 1 of operation respectively.

[0055] Drawing 20 is the plan of the semiconductor device in which the form 3 of implementation of this invention is shown, and drawing 19 is a cross section in the F-F cross section shown in drawing 20 . With reference to drawing 20 , the channel cut layer 113 is formed in the bottom of the separation insulator layer 4 of a pMOS field, and the channel cut layer 114 is formed in the bottom of the separation insulator layer 4 of a nMOS field. And the wiring 94 for fixing the potential of the impurity layer 122 is common to a pMOS field and a nMOS field, and should just be formed at least one. Moreover, potential is being fixed through wiring linked to the impurity range 111 of each conductivity type through the channel cut layers 113 and 114, respectively like the structure of the form 1 of operation which showed the channel formation fields 120 and 130 in drawing 3 .

[0056] Next, operation is explained. With reference to drawing 19 , by impressing about [0V] voltage, a channel is formed and, in VG=1.8V, VD=1.8V, VS=0V, and the channel formation field 130, the voltage impressed to each electrode operates by nMOS. Moreover, in pMOS, by impressing about [1.8V] voltage to VG=0-1.8V, VD=0-1.8V, VS=1.8V, and the channel formation field 120, a channel is formed and current flows. Moreover, about 4V is impressed to 0V and the impurity layer 122 in the channel cut layer 113 at 1.8V and the channel cut layer 114, respectively. such voltage -- the need -- responding -- a pressure up -- or the pressure may be lowered Such voltage is examples and is changed by gate insulation thickness or gate length.

[0057] Drawing 21 is a graph which shows the leakage current of the semiconductor device concerning the gestalt 3 of implementation of this invention, in the semiconductor device shown in drawing 19 , sets width of face of 0.4 micrometers and the separation insulator layer 4 to 0.2 micrometers for the thickness of 0.15 micrometers and the embedded oxide film 2, and carries out the simulation of the thickness of the semiconductor layer 3. In this graph, the leakage current which generated the source drain fields 74 and 75 of the transistor which adjoins through the separation insulator layer 4, and the potential difference generated between 82 and 83 in a horizontal axis and during this period is taken along a vertical axis. Among drawing, when, as for O, the impurity layer 122 is not formed, ** expresses with the impurity layer 122 the case where 4V are impressed, respectively. This drawing shows that a leakage current decreases remarkably and pressure-proofing's is improving by forming the impurity layer 122.

[0058] In the gestalt of this operation, although drawing where the impurity layer 122 was formed in the whole surface explained, if the impurity layer 122 is formed only in the lower part of the portion for which partialness STI is used as isolation, it can raise a separation property. Moreover, although an example of the portion which a nMOS transistor and a pMOS transistor adjoin was explained, the same is said of diode and all can be applied to the portion to which the potential difference is born by the portion which the impurity range of the reverse conductivity type of two transistors adjoins through the separation insulator layer of partialness STI structure by circuit arrangement here, for example. Drawing 22 is the cross section showing another semiconductor device concerning the gestalt 3 of implementation of this invention, and, for n type impurity range and 86, as for an insulator layer and 52, barrier metal, and 96 and 97 are [76 / p type impurity range and 51] wiring in drawing. When diode adjoins and is formed with reference to drawing, the channel cut layer 113 is adjoined, p type impurity range 84 is formed, the channel cut layer 114 is adjoined, n type impurity range 74 is formed, and it is controlled by the wiring 96 and 97 which each impurity range connects through the barrier metal 52. Furthermore, although the composition of a circuit explains wiring like the gestalt 1 of operation using the semiconductor device with which the number of layers of the layer insulation film formed between transistors differs from arrangement etc., and one transistor was formed in one active region, it is not restricted to especially this.

[0059] According to the semiconductor device shown in the gestalt 3 of this operation, it sets in SOI structure. Two or more pMOS transistors and nMOS transistors are formed every through the separation insulator layer of partialness STI structure. When the potential of the channel formation field 10 is being fixed in common in each field, while forming a semiconductor substrate and the impurity layer of a reverse conductivity type in the semiconductor substrate front face under an embedded oxide film In the portion which a nMOS transistor and a pMOS transistor adjoin Since p type and an n type channel cut layer are arranged so that the relation to pnpn with the impurity range of a transistor may become, and potential is fixed under a separation insulator layer, Even if the potential difference occurs between the impurity ranges of the reverse conductivity type of the transistor which adjoins through the separation insulator layer of partialness STI structure, while suppressing generating of the leakage current in this portion Pressure-proofing can be made high, and even if it turns minutely, the semiconductor device whose separation property improved can be obtained. Furthermore, when a pMOS transistor and a nMOS transistor adjoin and are formed, When the impurity layer 122 is prolonged and formed not only in the bottom of a separation insulator layer but in the bottom of the source drain fields 73, 74, and 83 and 84 Since it will be incorporated by the impurity layer 122

even if the impurity poured in on the occasion of source drain field formation runs through the embedded oxide film 2 and reaches even the semiconductor substrate 1, there is no possibility of becoming the cause of a circuit malfunction, and the effect that the reliability of a semiconductor device improves is done so.

[0060] Next, the manufacture method of the semiconductor device concerning the gestalt 3 of implementation of this invention is explained. Drawing 23 and drawing 24 are the cross sections showing one process of the manufacture method of a semiconductor device which shows the gestalt 3 of operation, and 301 is a photoresist mask in drawing 23 . First, the ion implantation of the impurity of n types, such as Lynn, is carried out like the gestalt 1 of operation from on the front face of the SOI substrate equipped with the embedded oxide film 2 and the semiconductor layer 3 on the front face of the semiconductor substrate 1, and the impurity layer 122 is formed in the portion to which the semiconductor substrate 1 touches the embedded oxide film 2. Next, like the gestalt 1 of operation, after forming the separation insulator layer 4 in an isolation region, on the separation insulator layer of a pMOS field, the photoresist mask 301 which has opening is formed, the ion implantation of the n type impurities, such as Lynn, is carried out to the whole surface in 110-130KeV and about two 1x1013 to 5x1013-/cm, and the channel cut layer 113 is formed. Drawing 23 is the cross section showing the element of the semiconductor device in the stage which this process finished.

[0061] Drawing 24 is the cross section showing one process of the manufacture method of a semiconductor device which shows the form 3 of operation, and 302 is a photoresist mask in drawing. After removing the photoresist mask 301 with reference to drawing, the photoresist mask 302 which has opening is formed on the separation insulator layer of a nMOS field, the ion implantation of the p type impurities, such as boron, is carried out to the whole surface in 30-50KeV and about two 5x1012 to 1x1013-/cm, and the channel cut layer 114 is formed. Drawing 24 is the cross section showing the element of the semiconductor device in the stage which this process finished. In the form 1 of operation, although the channel cut layer 11 was formed in advance of formation of the separation insulator layer 4, after forming the separation insulator layer 4, a channel cut layer is formed in the form 3 of this operation.

[0062] And like the form 1 of operation, after forming the silicon oxide by thermal oxidation in the whole surface (not shown) Form in a pMOS field the photoresist mask which has opening (not shown), and the ion implantation of Lynn or which arsenic n type impurity is carried out to the whole surface in 10-20KeV and about two 1x1012 to 5x1012-/cm. The impurity which adjusts threshold voltage to the channel formation field 120 is introduced, and this photoresist mask is removed (not shown). Then, the photoresist mask which has opening is formed in a nMOS field (not shown), the ion implantation of the p type impurities, such as boron and fluoridation boron, is carried out to the whole surface in 10-20KeV and about two 1x1012 to 5x1012-/cm, the impurity which adjusts a threshold to the channel formation field 130 is introduced, and this photoresist mask is removed (not shown).

[0063] Next, the gate insulator layer 5, the gate electrode 6, the source drain fields 72, 73, 82, and 83 of a pMOS field, the source drain fields 74, 75, 84, and 85 of a nMOS field, a sidewall 13, the layer insulation films 14 and 141, contact holes 15 and 151, and wiring 9 and 91 are formed like the form 1 of operation. Thus, the semiconductor device shown in drawing 19 is formed. Each contact hole and wiring can change formation sequence like the form 1 of operation if needed, and a further different layer insulation film and further different wiring are formed in the upper layer, and they may turn into a multilayer interconnection. [including the contact hole or wiring which are not shown in this drawing]

[0064] While being able to form the impurity layer 122 in semiconductor substrate 1 front face of the semiconductor device of the SOI structure which consists of the semiconductor substrate 1, an embedded oxide film 2, and a semiconductor layer 3 according to the manufacture method of the semiconductor device shown in the gestalt 3 of this operation An n type channel cut layer can be formed in the bottom of the separation insulator layer which separates the formed pMOS transistors. Under the separation insulator layer which can form an n type CHARU cut layer in the bottom of the separation insulator layer which separates pMOS transistors, and separates a pMOS transistor and a nMOS transistor p type and an n type channel cut layer can be formed so that the relation to pnpn with the impurity range of a transistor may become. And by fixing the potential of this impurity layer 122 and p type, and an n type channel cut layer, respectively It being common to each and fixing the potential of the channel formation field 10 of a pMOS transistor and a nMOS transistor Even if the potential difference occurs between the source drain fields of the pMOS transistor which adjoins through the separation insulator layer of partialness STI structure, and a nMOS transistor, while suppressing generating of the leakage current in this portion Pressure-proofing can be made high, and even if it turns minutely, the manufacture method of the semiconductor device whose separation property improved can be acquired. Furthermore, since the impurity layer 122 can be formed even not only in an isolation region but in the bottom of an active region when a pMOS transistor and a nMOS transistor adjoin and are formed, Since it incorporates in the impurity layer 122 and voltage is impressed, even if the impurity by which the ion implantation was carried out on the occasion of source drain field formation runs through the embedded oxide film 2 and reaches even the semiconductor substrate 1, There is no possibility of becoming the cause of a circuit malfunction, and the manufacture method of a semiconductor device which improved can be acquired.

[0065] Gestalt 4. drawing 25 of operation is the plan of the semiconductor device concerning the gestalt 4 of implementation of this invention. With reference to drawing, two or more sorts of different functional block on one semiconductor chip is formed in the semiconductor device concerning the gestalt 4 of this operation, and high integration and improvement in the speed are attained. And especially the thing in which control circuits, such as DRAM and a microprocessor (Micro Processor), are formed in this way is called mixed loading DRAM. Next, work of each functional block is explained. The data incorporated from the outside through the I/O section (I/O) section are controlled by the microprocessor section, and it is the

DSP (Digital Signal Processing) section, and high-speed processing is performed or they are read [are memorized or carried out in the DRAM section, and] from the DRAM section. At this time, the 1st cache array (First Cache Array) section synchronizes the digital data taken out from the DRAM section to the microprocessor section, and passes, or carries out the work which the data which finished processing are synchronized to the DRAM section, and passes them in the microprocessor section. And the 2nd cache array (Second Cache Array) section synchronizes an exchange of the data between the DSP section, the 1st cache array section, the microprocessor section, and the I/O section with each block, and has mediated it.

[0066] With each functional block, the portion with the need of fixing the potential of a channel formation field in common is equipped with the transistor indicated to the form 1 of operation, or 3 according to the function, and the impurity layer according to it, and it does not need to be the same about the structure of a source drain field, the conductivity type of an impurity layer, and the voltage impressed. Here, although an example of functional block is shown, it is not restricted only to this combination and may have the transistor shown only in the part only one in functional block indicated the form 1 of operation, or 3, the transistor which may be equipped with the impurity layer according to it, and was shown in the form 1 of operation, or 3 about all the functional block, and the impurity layer according to it.

[0067] In the semiconductor device with which two or more functional block was formed according to the semiconductor device concerning the form 4 of this operation in functional block Into a portion with the need of fixing in common, the potential of a channel formation field Since the conductivity type and the voltage to impress of the impurity layer which the 1st and 2nd active elements separated by partialness STI were formed according to the function needed, and was doubled with it can be determined, while attaining detailed-ization A leakage current is suppressed and the semiconductor device equipped with functional block whose separation pressure-proofing improved can be obtained.

[0068]

[Effect of the Invention] Since this invention is constituted as explained above, it does the following effects so. this invention can make pressure-proofing high, and even if it turns minutely, it does so the effect that the semiconductor device whose separation property improved can obtain, while being able to suppress generating of the leakage current in this portion in the semiconductor device of the SOI structure have partialness STI structure as an isolation construction even if the potential difference occurs between the transistors which adjoin through a separation insulator layer, since an impurity layer forms in a semiconductor substrate front face.

[0069] Furthermore, the MOS transistor which adjoins through the separation insulator layer of partialness STI structure has the same conductivity type. When being formed so that the source drain field may reach to an embedded oxide film Since the voltage clamp of the impurity layer of a semiconductor substrate front face is formed and carried out by the transistor and the reverse conductivity type while fixing the potential of the channel cut layer under a separation insulator layer, Even if the potential difference occurs between the source drain fields of the transistor which adjoins through a separation insulator layer, while being able to suppress generating of the leakage current in this portion, pressure-proofing can be made high, and even if it turns minutely, the semiconductor device whose separation property improved can be obtained.

[0070] Moreover, it sets to the MOS transistor of the same conductivity type formed so that the source drain field which adjoins through the separation insulator layer of partialness STI structure might reach to an embedded oxide film. While being able to arrange mutual threshold voltage with a sufficient precision by making the channel formation field of the adjoining transistor into floating, and sharing it, without fixing the potential of the channel cut layer under a separation insulator layer Since the voltage clamp of a transistor and the impurity layer of a reverse conductivity type is formed and carried out to the semiconductor substrate front face under a separation insulator layer, Even if the potential difference occurs between the source drain fields of the transistor which adjoins through a separation insulator layer, while being able to suppress generating of the leakage current in this portion, pressure-proofing can be made high, and even if it turns minutely, the semiconductor device whose separation property improved can be obtained.

[0071] Moreover, the MOS transistor which adjoins through the separation insulator layer of partialness STI structure has the same conductivity type. When being formed so that the source drain field may not reach to an embedded oxide film By forming the impurity layer of a semiconductor substrate front face by the same conductivity type as the source drain field of a transistor, and impressing the voltage which is a reverse bias to a semiconductor substrate Even if the potential difference occurs between the source drain fields of the transistor which adjoins through a separation insulator layer, while being able to suppress generating of the leakage current in this portion, pressure-proofing can be made high, and even if it turns minutely, the semiconductor device whose separation property improved can be obtained.

[0072] Moreover, when the impurity range of the transistor formed through the separation insulator layer of partialness STI structure is a reverse conductivity type in SOI structure, while forming a semiconductor substrate and the impurity layer of a reverse conductivity type in the semiconductor substrate front face under an embedded oxide film Since p type and an n type channel cut layer are arranged so that the relation to pnpn with the impurity range of a transistor may become, and potential is fixed under a separation insulator layer, Even if the potential difference occurs between the impurity ranges of the reverse conductivity type of the transistor which adjoins through a separation insulator layer, while suppressing generating of the leakage current in this portion, pressure-proofing can be made high, and even if it turns minutely, the semiconductor device whose separation property improved can be obtained.

[0073] Moreover, in SOI structure, diode is formed through the separation insulator layer of partialness STI structure. When the impurity range which adjoins through a separation insulator layer is a reverse conductivity type, while forming a semiconductor substrate and the impurity layer of a reverse conductivity type in the semiconductor substrate front face under

an embedded oxide film Since p type and an n type channel cut layer are arranged so that the relation to pnpn with the impurity range of diode may become, and potential is fixed under a separation insulator layer, Even if the potential difference occurs between the impurity ranges of the reverse conductivity type of the diode which adjoins through a separation insulator layer, while suppressing generating of the leakage current in this portion, pressure-proofing can be made high, and even if it turns minutely, the semiconductor device whose separation property improved can be obtained.

[0074] Furthermore, since it is characterized by to have been prolonged an impurity layer under an active region, and it is incorporated by the impurity layer and a voltage clamp is carried out to it even if the impurity poured in on the occasion of source drain field formation runs through an embedded oxide film and reaches even a semiconductor substrate by the impurity layer formed in a semiconductor substrate front face, there is no possibility may become the cause of a circuit malfunction, and the effect that the reliability of a semiconductor device improves does so.

[0075] in addition, in the semiconductor device with which two or more functional block was formed, the potential of a channel formation field into a portion with the need of fixing in common, in functional block Since the conductivity type and the voltage to impress of the impurity layer which the transistor separated by partialness STI was formed according to the function needed, and was doubled with it can be determined, while attaining detailed-ization A leakage current is suppressed and the semiconductor device equipped with functional block which improved can be obtained.

[0076] Moreover, since an impurity layer is formed in the semiconductor substrate front face of the semiconductor device of SOI structure and the wiring which fixes the potential of this impurity layer is formed, Even if the potential difference occurs between the impurity ranges of the transistor formed in the semiconductor layer front face through the separation insulator layer of partialness STI structure, while being able to suppress generating of the leakage current in this portion Pressure-proofing can be made high, and even if it turns minutely, the manufacture method of the semiconductor device whose separation property improved can be acquired. Furthermore, since it incorporates in an impurity layer even if the impurity by which the ion implantation was carried out runs through an embedded oxide film and reaches even a semiconductor substrate in case it is impurity-range formation since an impurity layer can be formed even not only in an isolation region but in the bottom of an active region, there is no possibility of becoming the cause of a circuit malfunction, and the manufacture method of a semiconductor device which improved can be acquired.

[0077] Furthermore, since the ion implantation of the high-concentration impurity is carried out to the semiconductor layer under a separation insulator layer rather than a semiconductor layer and the channel cut layer is formed, the semiconductor device whose separation property improved further can be obtained.

[0078] moreover, when the pMOS transistor and the nMOS transistor adjoin through the separation insulator layer of STI structure It can arrange so that one side of each source drain field and the channel cut layer formed in the bottom of a separation insulator layer may serve as pnpn. By fixing the potential of this impurity layer and p type, and an n type channel cut layer, respectively Even if the potential difference occurs between the source drain fields of the transistor which adjoins through a separation insulator layer, while suppressing generating of the leakage current in this portion, pressure-proofing can be made high, and even if it turns minutely, the manufacture method of the semiconductor device whose separation property improved can be acquired.

[0079] Moreover, since an impurity layer is formed in the semiconductor substrate front face of the semiconductor device of SOI structure and the wiring which fixes the potential of this impurity layer is formed, Even if the potential difference occurs between the impurity ranges of the transistor formed in the semiconductor layer front face through the separation insulator layer of partialness STI structure, while being able to suppress generating of the leakage current in this portion Pressure-proofing can be made high, and even if it turns minutely, the manufacture method of the semiconductor device whose separation property improved can be acquired.

[0080] Furthermore, since the ion implantation of the high-concentration impurity is carried out to the semiconductor layer under a separation insulator layer rather than a semiconductor layer and the channel cut layer is formed, the semiconductor device whose separation property improved further can be obtained.

[Translation done.]